Abstract of the Disclosure

An embodiment of this invention pertains to a wire that interconnects multiple function blocks within a programmable logic device ("PLD"). An electrically optimum physical length is determined for the wire. A wire having the electrically optimum physical length transmits a signal down the wire as fast as possible. Some of the wires used in the PLD have a physical length substantially the same as the electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations. The physical length, as used herein, is the measured length of the wire. A logical length of the wire, as used herein, is the number of function blocks that the wire spans. Given that the function blocks have a different height and width, the logical length of the wire varies depending on the orientation of the wire.

A routing architecture is an array that includes rows and columns of function blocks. The columns of the array are connected with horizontal lines ("H-line") and the rows of the array are connected with vertical lines ("V-line). The types of H-lines include a H4 line that spans four function blocks, a H8 line that spans eight function blocks, and a H24 line that spans twenty-four function blocks. The types of V-lines include a V4 line that spans four function blocks, a V8 line that spans eight function blocks, and a V16 line that spans sixteen function blocks.